

# SANYO Semiconductors DATA SHEET



## CMOS IC FROM 64K byte, RAM 2048 byte on-chip 8-bit 1-chip Microcontroller

#### Overview

The SANYO LC87F5M64A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 64K-byte flash ROM (onboard programmable), 2048-byte RAM, On-chip debugging function, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two UART ports (full duplex), an 8-bit 11-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, and a 27-source 10-vector interrupt feature.

### Features

#### ■Flash ROM

- Capable of on-board-programing with wide range, 2.7 to 5.5V, of voltage source
- Block-erasable in 128 byte units
- 65536 × 8 bits

#### ■RAM

- 2048 × 9 bits
- ■Minimum Bus Cycle Time
  - 83.3ns (12MHz) V<sub>DD</sub>=2.8 to 5.5V
  - 125ns (8MHz) V<sub>DD</sub>=2.5 to 5.5V
  - 500ns (2MHz) V<sub>DD</sub>=2.2 to 5.5V
  - Note: The bus cycle time here refers to the ROM read speed.

#### ■Minimum Instruction Cycle Time (tCYC)

- 250ns (12MHz) V<sub>DD</sub>=2.8 to 5.5V
- 375ns (8MHz) V<sub>DD</sub>=2.5 to 5.5V
- $1.5\mu s (2MHz)$  VDD=2.2 to 5.5V

#### ■Ports

- Normal withstand voltage I/O ports
   Ports whose I/O direction can be designated in 1-bit units
   46 (P1n, P2n, P3n, P70 to P73, P80 to P86, PCn,
  - Ports whose I/O direction can be designated in 4-bit units
- Normal withstand voltage input port
- Dedicated oscillator ports
- Reset pins
- Power pins

46 (P1n, P2n, P3n, P70 to P73, P80 to P86, PCn, PWM2, PWM3, XT2) 8 (P0n)

1 (XT1) 2 (<u>CF1</u>, CF2) 1 (RES) 6 (V<sub>SS</sub>1 to 3, V<sub>DD</sub>1 to 3)

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# SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

#### ■Timers

- Timer 0: 16-bit timer/counter with a capture register
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) ×2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)
    - + 8-bit counter (with an 8-bit capture register)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler  $\times$  2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)
    - (toggle outputs also possible from the lower-order 8-bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  - 2) Interrupts programmable in 5 different time schemes.

#### ■High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 24MHz (at a main clock of 12MHz).
- 2) Can generate output real-time.

#### ■SIO

- SIO0: 8-bit synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- ■UART: 2 channels
  - Full duplex
  - 7/8/9 bit data bits selectable
  - 1 stop bit (2 bit in continuous data transmission)
  - Built-in baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)
- ■AD Converter: 8 bits × 11 channels
- ■PWM: Multifrequency 12-bit PWM × 2 channels

Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- 1) Noise filtering function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
- 2) The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.
- ■Watchdog Timer
  - External RC watchdog timer
  - Interrupt and reset signals selectable

■Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

#### ■Interrupts

- 27 sources, 10 vector addresses
  - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INTO
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer0/base timer1
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/UART2 receive
8	0003BH	H or L	SIO/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 1024 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions

- 16-bits × 8-bits (5 tCYC execution time)
- 24-bits × 16-bits (12 tCYC execution time)
- 16-bits ÷ 8-bits (8 tCYC execution time)
- 24-bits ÷ 16-bits (12 tCYC execution time)

■Oscillation Circuits

• CF oscillation circuit

- RC oscillation circuit (internal)
- : For system clock
- : For system clock, with internal Rf
- Crystal oscillation circuit
- : For low-speed system clock • Multifrequency RC oscillation circuit (internal) : For system clock

System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 250ns, 500ns, 1.0µs, 2.0µs, 4.0µs, 8.0µs, 16.0µs, 32.0µs, and 64.0µs (at a main clock rate of 12MHz).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The CF, RC, and crystal oscillators automatically stop operation.
  - 2) There are three ways of resetting the HOLD mode.
    - (1) Setting the reset pin to the lower level.
    - (2) Setting at least one of the INTO, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  - 1) The CF and RC oscillators automatically stop operation.
  - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  - 3) There are four ways of resetting the X'tal HOLD mode.
    - (1) Setting the reset pin to the low level
    - (2) Setting at least one of the INTO, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
    - (4) Having an interrupt source established in the base timer circuit
- ■On-chip Debugger Function

• Permits software debugging with the test device installed on the target board.

- ■Package Form
  - QIP64E  $(14 \times 14)$  : "Lead-free type"
- Development Tools
  - Evaluation (EVA) chip
     Emulator
     EVA62S + ECB876600D + SUB875M00 + POD64QFP ICE-B877300 + SUB875M00 + POD64QFP
  - On-chip-debugger : TCB87-TypeB + LC87F5M64A

■Programming Boards

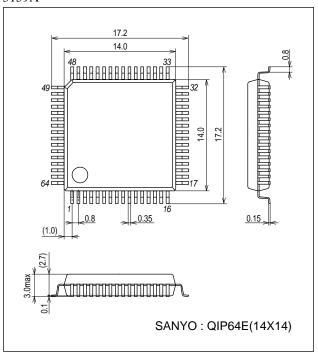
u u	
Package	Programming boards
QIP64E(14 × 14)	W87F50256Q

#### ■Flash ROM Programmer

Maker	Model	Support version(Note)	Device
Flash Support Group, Inc.(Single)	AF9708/09/09B (including product of Ando Electric Co.,Ltd)	Revision : After Rev.02.73	LC87F6D64A
Flash Support	AF9723(Main body) (including product of Ando Electric Co.,Ltd)	-	-
Group, Inc.(Gang)	AF9833(Unit) (including product of Ando Electric Co.,Ltd)	-	-
SANYO	SKK/SKK Type-B/SKK DBG Type-B (SANYO FWS)	Application Version: After 1.04 Chip Data Version: After2.10	LC87F5M64A

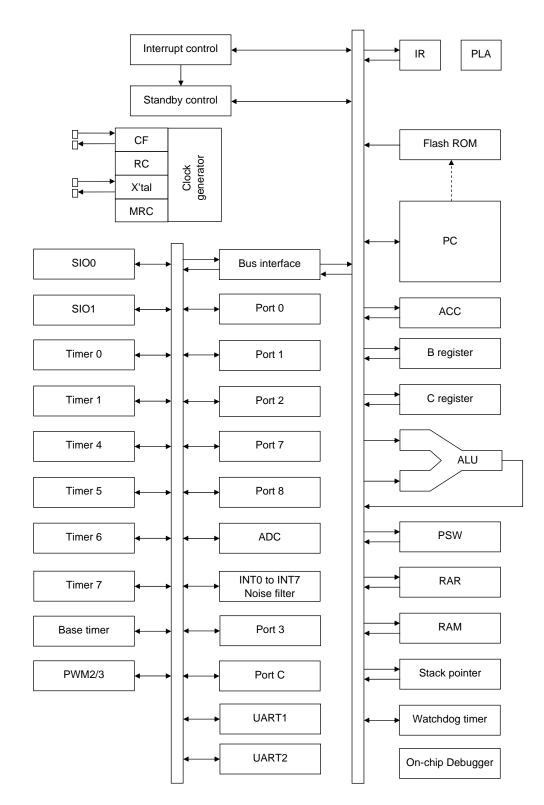
#### **Package Dimensions**

unit : mm (typ) 3159A



#### **Pin Assignment** PC7/DBGP2 PC5/DBGP0 PC6/DBGP1 P83/AN3 P84/AN4 P85/AN5 P86/AN6 VDD3 VSS<sup>3</sup> PC2 ЪЗ PCO PC PC4 P30 P31 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 P70/INT0/T0LCP/AN8 49 32 🗌 P32/UTX1 P71/INT1/T0HCP/AN9 50 🗋 P33/URX1 31 P72/INT2/T0IN/NKIN 51 30 P34/UTX2 P73/INT3/T0IN 52 29 \_\_\_\_\_ P35/URX2 RES 53 28 🗆 P36 XT1/AN10 54 27 🗆 P37 XT2/AN11 🔤 55 P27/INT5/T1IN 26 P26/INT5/T1IN 25 VSS1 □56 LC87F5M64A CF1 57 24 P25/INT5/T1IN CF2 58 23 P24/INT5/T1IN/INT7 22 P23/INT4/T1IN V<sub>DD</sub>1 ∐59 P80/AN0 60 P22/INT4/T1IN 21 P21/INT4/T1IN P81/AN1 61 20 P82/AN2 62 19 P20/INT4/T1IN/INT6 P10/SO0 63 18 D P07/T7O P11/SI0/SB0 64 17 P06/T6O 5 6 7 8 9 10 11 12 13 14 15 16 1 2 3 4 P12/SCK0 P05/CKO P17/T1PWMH/BUZ [ PWM2 [ PWM3 VDD2 VSS<sup>2</sup> POO P02 | P03 | P04 | P13/S01 P14/SI1/SB1 P15/SCK1 P16/T1PWML P01 Top view SANYO: QIP64E(14×14) "Lead-free Type"

## System Block Diagram



# Pin Description

Pin Name	I/O			Des	scription			Ор	tion
V <sub>SS</sub> 1, V <sub>SS</sub> 2 V <sub>SS</sub> 3	-	- Power supply p	bin					Ν	lo
V <sub>DD</sub> 1, V <sub>DD</sub> 2 V <sub>DD</sub> 3	-	+ Power supply	pin					Ν	<b>l</b> o
Port 0	I/O	• 8-bit I/O port						Y	es
P00 to P07		<ul> <li>I/O specifiable</li> </ul>	in 4-bit units						
		<ul> <li>Pull-up resistor</li> </ul>	can be turned	on and off in 4-bi	t units				
		HOLD release	input						
		Port 0 interrupt	input						
		<ul> <li>Shared Pins</li> </ul>							
				ck/can selected f	rom sub clock)				
		P06: Timer 6 to							
		P07: Timer 7 to	oggle output						
Port 1	I/O	8-bit I/O port						Y	es
P10 to P17		I/O specifiable							
		Pull-up resistor	can be turned	on and off in 1-bi	t units				
		Pin functions							
		P10: SIO0 data	•						
		P11: SIO0 data	•						
		P12: SIO0 cloc							
		P13: SIO1 data	-						
		P14: SIO1 data	•						
		P15: SIO1 cloc							
		P16: Timer 1 P	WMH output/be						
Port 2	I/O	8-bit I/O port						v	es
	1/0	• I/O specifiable	in 1-bit unite					'	63
P20 to P27		Pull-up resistor		on and off in 1-bi	t unite				
		Other functions			t units				
				put/timer 1 even	t input/timer 01 o	capture input/			
				T6 input/timer 01	•	• •			
			• •	reset input/timer	• •		/uqu		
			capture input	· · · · · · · · · · · · · · · · · · ·					
				put/timer 1 even	t input/timer 0L o	capture input/			
		-		T7 input/timer 0I					
		P25 to P27: IN	T5 input/HOLD	reset input/timer	1 event input/tin	ner 0L capture ir	nput/		
		timer 0H	capture input						
		Interrupt acknow	wledge type						
			Rising	Falling	Rising/	H level	L level		
					Falling		2.0.0.		
		INT4	enable	enable	enable	disable	disable		
		INT5	enable	enable	enable	disable	disable		
		INT6	enable	enable	enable	disable	disable		
	1	INT7	enable	enable	enable	disable	disable		

Continued on next page.

Pin Name	I/O			Des	cription			Option
Port 7	I/O	4-bit I/O port						No
P70 to P73		<ul> <li>I/O specifiable i</li> </ul>	n 1-bit units					
		Pull-up resistor	can be turned of	on and off in 1-bi	t units			
		<ul> <li>Shared Pins</li> </ul>						
		P70: INT0 input	/HOLD reset in	put/timer 0L capt	ure input/watcho	dog timer output		
		P71: INT1 input	HOLD reset in	put/timer 0H cap	ture input			
		P72: INT2 input	/HOLD reset in	put/timer 0 event	input/timer 0L c	apture input/		
		high spee	d clock counter	input				
		P73: INT3 input	t (with noise filte	er)/timer 0 event	input/timer 0H ca	apture input		
		AD converter in	put port: AN8 (I	P70), AN9 (P71)				
	Interrupt acknowledge type							
			Rising	Falling	Rising/ Falling	H level	L level	
		INT0	enable	enable	disable	enable	enable	
		INT1	enable	enable	disable	enable	enable	
		INT2	enable	enable	enable	disable	disable	
		INT3	enable	enable	enable	disable	disable	
Port 8	I/O	• 7-bit I/O port						No
P80 to P86		<ul> <li>I/O specifiable i</li> </ul>	n 1-bit units					
		Shared Pins						
		AD converter in	put port : AN0 (	P80) to AN6 (P8	6)			
PWM2	I/O	PWM2 and PW	M3 output ports	3				No
PWM3		General-purpos	e I/O available					
Port 3	I/O	8-bit I/O port						Yes
P30 to P37		• I/O specifiable i	n 1-bit units					
		Pull-up resistor	can be turned of	on and off in 1-bi	t units			
		<ul> <li>Pin functions</li> </ul>						
		P32: UART1 tra	ansmit					
		P33: UART1 re	ceive					
		P34: UART2 tra	ansmit					
		P35: UART2 re	ceive					
Port C	I/O	<ul> <li>8-bit I/O port</li> </ul>						Yes
PC0 to PC7		<ul> <li>I/O specifiable i</li> </ul>	n 1-bit units					
		<ul> <li>Pull-up resistor</li> </ul>	can be turned of	on and off in 1-bi	t units			
		<ul> <li>Pin functions</li> </ul>						
			P2(PC5 to PC7	'): On-chip Debu	gger			
RES	Input	Reset pin						No
XT1	Input	<ul> <li>32.768kHz crys</li> </ul>	tal oscillator inp	out pin				No
		<ul> <li>Shared pins</li> </ul>						
		General-purpos						
		AD converter in						
		Must be connec						
XT2	I/O	• 32.768kHz crys	tal oscillator inp	out pin				No
		Shared pins						
		General-purpos	-					
		AD converter in						
0.57				kept open if not t	o be used.			
CF1	Input	Ceramic resonat						No
CF2	Output	Ceramic resonat	or output pin					No

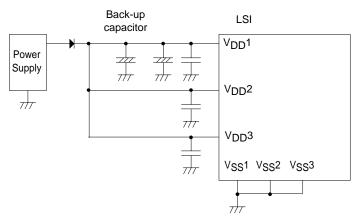
### **Port Output Types**

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

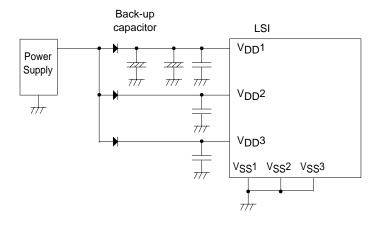
Port	Options Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P86	-	No	Nch-open drain	No
PWM2, PWM3	-	No	CMOS	No
P30 to P37	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PC0 to PC7	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
XT1	-	No	Input for 32.768kHz crystal oscillator (Input only)	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

<sup>(</sup>Example 1) When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



(Example 2) The high-level output at the ports is unstable when the HOLD mode backup is in effect.



<sup>\*1:</sup> Make the following connection to minimize the noise input to the V<sub>DD</sub>1 pin and prolong the backup time. Be sure to electrically short the V<sub>SS</sub>1, V<sub>SS</sub>2, and V<sub>SS</sub>3 pins.

## **Absolute Maximum Ratings** at $Ta = 25^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

	Parameter	Symbol	Pins/Remarks	Conditions	1	 	Speci	fication	
		-			V <sub>DD</sub> [V]	min	typ	max	uni
	ximum supply tage	V <sub>DD</sub> max	V <sub>DD</sub> 1, V <sub>DD</sub> 2, V <sub>DD</sub> 3	V <sub>DD</sub> 1=V <sub>DD</sub> 2=V <sub>DD</sub> 3		-0.3		+6.5	
np	ut voltage	V <sub>I</sub> (1)	XT1, CF1			-0.3		V <sub>DD</sub> +0.3	
np	ut/Output voltage	V <sub>IO</sub> (1)	Ports 0, 1, 2 Ports 7, 8 Ports 3, C PWM0, PWM1, XT2			-0.3		V <sub>DD</sub> +0.3	V
	Peak output current	IOPH(1)	Ports 0, 1, 2 Ports 3, C	CMOS output select Per 1 application pin		-10			
		IOPH(2)	PWM2, PWM3	Per 1 application pin.		-20			
		IOPH(3)	P71 to P73	Per 1 application pin.		-5			
current	Mean output current	IOMH(1)	Ports 0, 1, 2 Ports 3, C	CMOS output select Per 1 application pin		-7.5			
	(Note1-1)	IOMH(2)	PWM2, PWM3	Per 1 application pin		-10			
ut cu		IOMH(3)	P71 to P73	Per 1 application pin		-3			
High level output current	Total output	ΣIOAH(1)	P71 to P73	Total of all applicable pins		-10			
	current	ΣIOAH(2)	Ports, 1 PWM2, PWM3	Total of all applicable pins		-25			
Hig		ΣIOAH(3)	Ports 0, 2	Total of all applicable pins		-25			
		ΣIOAH(4)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins		-45			
		ΣIOAH(5)	Port 3	Total of all applicable pins		-25			
		ΣIOAH(6)	Ports C	Total of all applicable pins		-25			
		ΣIOAH(7)	Ports 3, C	Total of all applicable pins		-45			
	Peak output	IOPL(1)	P02 to P07	Per 1 application pin.					
	current		Ports 1, 2 Ports 3, C					20	
		IOPL(2)	PWM2, PWM3 P00, P01	Per 1 application pin.				20	m
		IOPL(2)	Pots 7, 8, XT2	Per 1 application pin.				30 10	
	Mean output current (Note1-1)	IOML(1)	P02 to P07 Ports 1, 2 Ports 3, C	Per 1 application pin.				15	
rrent	· · · ·		PWM2, PWM3						
curr		IOML(2)	P00, P01	Per 1 application pin.				20	
ıtput		IOML(3)	Ports 7, 8, XT2	Per 1 application pin.				7.5	
Low level output cu	Total output current	ΣIOAL(1)	Port 7 P83 to P86, XT2	Total of all applicable pins				15	
-ow		$\Sigma IOAL(2)$	P80 to P82	Total of all applicable pins				15	
_		ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins				20	
		ΣIOAL(4)	Ports 1 PWM2, PWM3	Total of all applicable pins				45	
		$\Sigma IOAL(5)$	Ports 0, 2	Total of all applicable pins				45	
		ΣIOAL(6)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins				80	
		$\Sigma IOAL(7)$	Port 3	Total of all applicable pins				45	
		ΣIOAL(8)	Ports C	Total of all applicable pins				45	
		ΣIOAL(9)	Ports 3, C	Total of all applicable pins				80	
	ximum power sipation	Pd max	QIP64E(14×14)	Ta=-40 to +85°C				300	m'
	erating ambient	Topr				-40		+85	°(
	orage ambient nperature	Tstg				-55		+125	-(

Note 1-1: The mean output current is a mean value measured over 100ms.

Deremeter	Cumhal	Dine/Demorka	Conditions			Specif	ication	
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Operating	V <sub>DD</sub> (1)	V <sub>DD</sub> 1=V <sub>DD</sub> 2=V <sub>DD</sub> 3	0.245µs≤ tCYC≤200µs		2.8		5.5	
supply voltage			0.367µs≤ tCYC≤200µs		2.5		5.5	
(Note2-1)			1.47µs≤ tCYC≤200µs		2.2		5.5	
Memory sustaining supply voltage	VHD	V <sub>DD</sub> 1=V <sub>DD</sub> 2=V <sub>DD</sub> 3	RAM and register contents sustained in HOLD mode		2.0		5.5	
High level input voltage	∨I <u>H</u> (1)	Ports 1, 2 P71 to P73 P70 port input/ interrupt side		2.2 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	
	V <sub>IH</sub> (2)	Ports 0, 8, 3, C PWM2, PWM3		2.2 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	
	V <sub>IH</sub> (3)	P70 watchdog timer side		2.2 to 5.5	0.9V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH</sub> (4)	XT1, XT2, CF1, RES		2.2 to 5.5	0.75V <sub>DD</sub>		V <sub>DD</sub>	
Low level input voltage	V <sub>IL</sub> (1)	Ports 1, 2 P71 to P73		4.0 to 5.5	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.4	
		P70 port input/ Interrupt side		2.2 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	Ports 0, 8, 3, C PWM2, PWM3		4.0 to 5.5	V <sub>SS</sub>		0.15V <sub>DD</sub> +0.4	
				2.2 to 5.5	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (3)	Port 70 watchdog timer side		2.2 to 4.0	V <sub>SS</sub>		0.8V <sub>DD</sub> -1.0	
	V <sub>IL</sub> (4)	XT1, XT2, CF1, RES		2.2 to 5.5	VSS		0.25V <sub>DD</sub>	
Instruction cycle	tCYC			2.8 to 5.5	0.245		200	
time				2.5 to 5.5	0.367		200	μs
(Note2-2)				2.2 to 5.5	1.47		200	
External system	FEXCF(1)	CF1	CF2 pin open	2.8 to 5.5	0.1		12	
clock frequency			System clock frequency	2.5 to 5.5	0.1		8	
			<ul> <li>division rate=1/1</li> <li>External system clock duty=50±5%</li> </ul>	2.2 to 5.5	0.1		2	MH
			CF2 pin open	2.8 to 5.5	0.2		24.4	
			System clock frequency	2.5 to 5.5	0.1		16	
			division rate=1/2	2.2 to 5.5	0.1		4	
Oscillation frequency	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.8 to 5.5		12		
range (Note2-3)	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		4		MH
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation	2.5 to 5.5		16		
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.2 to 5.5		32.768		kHz

## **Recommended Operating Conditions** at $Ta = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Note 2-1: V<sub>DD</sub> must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Deremeter	Cumbal	Pins/Remarks	Conditions			Specific	ation	
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High level input current	I <sub>IH</sub> (1)	Ports 0, 1, 2 Ports 7, 8 Ports 3, C RES PWM2, PWM3	Output disabled Pull-up resistor off V <sub>IN</sub> =V <sub>DD</sub> (Including output Tr's off leakage current))	2.2 to 5.5			1	
	I <sub>IH</sub> (2)	XT1, XT2	For input port specification VIN=VDD	2.2 to 5.5			1	
	I <sub>IH</sub> (3)	CF1	V <sub>IN</sub> =V <sub>DD</sub>	2.2 to 5.5			15	Ι.
Low level input current	I <sub>IL</sub> (1)	Ports 0, 1, 2 Ports 7, 8 Ports 3, C RES PWM2, PWM3	Output disabled Pull-up resistor off VIN=VSS (Including output Tr's off leakage current))	2.2 to 5.5	-1			μA
	I <sub>IL</sub> (2)	XT1, XT2	For input port specification VIN <sup>=V</sup> SS	2.2 to 5.5	-1			
	I <sub>IL</sub> (3)	CF1	V <sub>IN</sub> =V <sub>SS</sub>	2.2 to 5.5	-15			
High level output	V <sub>OH</sub> (1)	Ports 0, 1, 2	I <sub>OH</sub> =-1mA	4.5 to 5.5	V <sub>DD</sub> -1			
voltage	V <sub>OH</sub> (2)	Ports 3, C	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (3)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (4)	Ports 71 to 73	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (5)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (6)	PWM2, PWM3	I <sub>OH</sub> =-10mA	4.5 to 5.5	V <sub>DD</sub> -1.5			
	V <sub>OH</sub> (7)		I <sub>OH</sub> =-1.6mA	3.0 to 5.5	V <sub>DD</sub> -0.4			v
	V <sub>OH</sub> (8)		I <sub>OH</sub> =-1mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
Low level output	V <sub>OL</sub> (1)	Ports 0, 1, 2	I <sub>OL</sub> =10mA	4.5 to 5.5			1.5	1
voltage	V <sub>OL</sub> (2)	Ports 3, C	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (3)	PWM2, PWM3,	I <sub>OL</sub> =1mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (4)	Ports 7, 8	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	1
	V <sub>OL</sub> (5)	XT2	I <sub>OL</sub> =1mA	2.2 to 5.5			0.4	1
	V <sub>OL</sub> (6)	P00, P01	I <sub>OL</sub> =30mA	4.5 to 5.5			1.5	1
	V <sub>OL</sub> (7)		I <sub>OL</sub> =5mA	3.0 to 5.5			0.4	1
	V <sub>OL</sub> (8)		I <sub>OL</sub> =2.5mA	2.2 to 5.5			0.4	1
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 7	V <sub>OH</sub> =0.9V <sub>DD</sub>	4.5 to 5.5	15	35	80	
	Rpu(2)	Ports 3, C		2.2 to 5.5	18	35	150	kΩ
Hysteresis voltage	VHYS	RES Ports 1, 2, 7		2.2to 5.5		0.1V <sub>DD</sub>		v
Pin capacitance	СР	All pins	<ul> <li>For pins other than that under test: V<sub>IN</sub>=V<sub>SS</sub></li> <li>f=1MHz</li> <li>Ta=25°C</li> </ul>	2.2 to 5.5		10		pF

## **Electrical Characteristics** at $Ta = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

## Serial I/O Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$ 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

P	Parameter Syr			Conditions	Specification			noation	
			/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 6.		2			
×	Low level pulse width	tSCKL(1)				1			
put cloc	High level pulse width	tSCKH(1)			2.2 to 5.5	1			101/0
ll		tSCKHA(1)		Continuous data transmission/reception mode     See Fig. 6.     (Note 4-1-2)		4			tCYC
	Frequency	tSCK(2)	SCK0(P12)	CMOS output selected     See Fig. 6.		4/3			
ck	Low level pulse width	tSCKL(2)					1/2		tSCK
itput clo	High level pulse width	tSCKH(2)			2.2 to 5.5		1/2		ISCK
Õ		tSCKHA(2)		<ul> <li>Continuous data transmission/reception mode</li> <li>CMOS output selected</li> <li>See Fig. 6.</li> </ul>		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Da	ta setup time	tsDI(1)	SI0(P11), SB0(P11)	<ul> <li>Must be specified with respect to rising edge of SIOCLK</li> <li>See fig. 6.</li> </ul>	2.2 to 5.5	0.03			
Da	ta hold time	thDI(1)			2.2 to 5.5	0.03			
clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11),	Continuous data transmission/reception mode (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.05	
Input		tdD0(2)		Synchronous 8-bit mode     (Note 4-1-3)	2.2 to 5.5			1tCYC +0.05	μS
Output clock		tdD0(3)		• (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.15	
	Input clock	Big     High level       Pulse width       pulse width       Low level       pulse width       High level       pulse width       Data setup time       Data hold time       Yoop ndel       Output       delay time	Note     High level     tSCKH(1)       Pulse width     tSCKHA(1)       tSCKHA(1)     tSCKHA(1)       tSCKHA(1)     tSCKHA(1)       tSCKHA(1)     tSCKHA(1)       tSCKHA(1)     tSCKHA(1)       tSCKHA(1)     tSCKHA(1)       tSCKHA(1)     tSCKHA(2)       tSCKHA(2)     tSCKHA(2)       tSCKHA(2)     tSCKHA(2)       tSCKHA(2)     tSCKHA(2)       tSCKHA(2)     tSCKHA(2)       tSCKHA(2)     tSCKHA(2)       tSCKHA(2)     tSCKHA(2)	Notest         High level pulse width         tSCKH(1)           Image: Second sec	Oppose         High level pulse width         tSCKH(1)         · Continuous data transmission/reception mode · See Fig. 6. · (Note 4-1-2)           Frequency         tSCK(2)         SCK0(P12)         · CMOS output selected · See Fig. 6. · (Note 4-1-2)           Low level pulse width         tSCKL(2)         · COntinuous data transmission/reception mode · See Fig. 6.           High level pulse width         tSCKH2)         · Continuous data transmission/reception mode · CMOS output selected · See Fig. 6.           Data setup time         tsDl(1)         SI0(P11), SB0(P11), Data hold time         SI0(P11, SB0(P11), SB0(P11), SB0(P11), Data hold time         · Continuous data transmission/reception mode · CMOS output selected · See Fig. 6.           Output         tdD0(1)         SO0(P10), SB0(P11), ItdD0(2)         · Continuous data transmission/reception mode · (Note 4-1-3)           vootput tidD0(3)         tdD0(1)         SO0(P10), SO(P10, SO(P10, Note 4-1-3)         · Continuous data transmission/reception mode · (Note 4-1-3)	NoteHigh level pulse widthtSCKH(1)·Continuous data transmission/reception mode ·See Fig. 6. ·(Note 4-1-2)2.2 to 5.5FrequencytSCK(2)SCK0(P12)·Continuous data transmission/reception mode ·See Fig. 6. ·(Note 4-1-2)·Contoreception mode ·See Fig. 6. ·(Note 4-1-2)	Note         High level pulse width         tSCKH(1)         Continuous data transmission/reception mode         2.2 to 5.5         1           Note         tSCKHA(1)         tSCKHA(1)         *Continuous data transmission/reception mode         *See Fig. 6.         4         4           Note         tSCK(2)         SCK0(P12)         *CMOS output selected         *See Fig. 6.         4         4/3           Low level         tSCKL(2)         *SCK0(P12)         *Continuous data transmission/reception mode         *See Fig. 6.         2.2 to 5.5         4/3           Use width         tSCKHA(2)         *Continuous data transmission/reception mode         *Continuous data         *See Fig. 6.         2.2 to 5.5         1           Data setup time         tsDl(1)         Sl0(P11), SB0(P11), SB0(P	000000000000000000000000000000000000	$ \frac{90}{90} \frac{9}{90} \frac{9}{90}$

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

#### 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

	Р	arameter	Symbol	Pins/	Conditions			Spec	ification	
	P	arameter	Symbol	Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
	×	Frequency	tSCK(3) SCK1(P15) • See Fig.		• See Fig. 6.		2			
	Input clock	Low level pulse width	tSCKL(3)			2.2 to 5.5	1			1010
clock	In	High level pulse width	tSCKH(3)				1			tCYC
Serial clock	ck	Frequency	tSCK(4)	SCK1(P15)	CMOS output selected.     See Fig. 6.		2			
	Output clock	Low level pulse width	tSCKL(4)		2		1/2			10.01/
	nO	High level pulse width	tSCKH(4)				1/2			tSCK
Serial input	Da	ta setup time	setup time tsDI(2) SI1(P <sup>2</sup>		SI1(P14)       • Must be specified with respect to         SB1(P14),       rising edge of SIOCLK         • See fig. 6.		0.03			
Serial	Da	ta hold time	thDI(2)			2.2 to 5.5	0.03			
Serial output	Ou tim	itput delay ie	tdD0(4)	SO1(P13), SB1(P14)	<ul> <li>Must be specified with respect to falling edge of SIOCLK</li> <li>Must be specified as the time to the beginning of output state change in open drain output mode.</li> <li>See Fig. 6.</li> </ul>	2.2 to 5.5			(1/3)tCYC +0.05	μs

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

# **Pulse Input Conditions** at $Ta = -40^{\circ}C$ to $+85^{\circ}C$ , VSS1 = VSS2 = VSS3 = 0V

Deremeter	Cumb ol	Pins/Remarks	Conditions			Speci	fication	
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High/low level	tPIH(1)	INT0(P70),	<ul> <li>Interrupt source flag can be set.</li> </ul>					
pulse width	tPIL(1)	INT1(P71),	<ul> <li>Event inputs for timer 0 or 1 are</li> </ul>					
		INT2(P72)	enabled.					
		INT4(P20 to P23),		2.2 to 5.5	1			
		INT5(P24 to P27),						
		INT6(P20)						
		INT7(P24)						tCYC
	tPIH(2)	INT3(P73) when noise filter	<ul> <li>Interrupt source flag can be set.</li> </ul>	2.2 to 5.5	2			
	tPIL(2)	time constant is 1/1.	• Event inputs for timer 0 are enabled.	2.2 10 5.5	Z			
	tPIH(3)	INT3(P73) when noise filter	<ul> <li>Interrupt source flag can be set.</li> </ul>	2.2 to 5.5	64			
	tPIL(3)	time constant is 1/32	• Event inputs for timer 0 are enabled.	2.2 10 5.5	64			
	tPIH(4)	INT3(P73) when noise filter	<ul> <li>Interrupt source flag can be set.</li> </ul>	2.2 to 5.5	256			
	tPIL(4) time constant is 1/128 • Event inputs for timer 0 are enabled.		2.2 to 5.5	256				
	tPIL(5)	RES	Resetting is enabled.	2.2 to 5.5	200			μS

# **AD** Converter Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

5	0.1.1					Specifi	cation	
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Resolution	Ν	AN0(P80) to		3.0 to 5.5		8		bit
Absolute accuracy	ET	AN6(P86), AN8(P70),	(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD	AN9(P71), AN10(XT1), AN11(XT2),	AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	11.74 (tCYC= 0.367μs)		97.92 (tCYC= 3.06μs)	
				3.0 to 5.5	23.53 (tCYC= 0.735μs)		97.92 (tCYC= 3.06μs)	
			AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.245μs)		97.92 (tCYC= 1.53μs)	μS
				3.0 to 5.5	23.49 (tCYC= 0.367μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN			3.0 to 5.5	V <sub>SS</sub>		V <sub>DD</sub>	V
Analog port	IAINH	]	VAIN=V <sub>DD</sub>	3.0 to 5.5			1	
input current	IAINL		VAIN=V <sub>SS</sub>	3.0 to 5.5	-1			μA

Note 6-1: The quantization error ( $\pm 1/2$  LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

#### **Consumption Current Characteristics** at $Ta = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	r				
raidiiielei	Symbol		Conditions	V <sub>DD</sub> [V]	min	min typ		unit
Normal mode consumption current	IDDOP(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3	FmCF=12MHz ceramic oscillation mode     FmX'tal=32.768kHz by crystal oscillation     mode	4.5 to 5.5		9.1	18.5	
(Note 7-1)			<ul> <li>System clock set to 12MHz side</li> <li>Internal RC oscillation stopped</li> <li>frequency variable RC oscillation stopped</li> <li>1/1 frequency division ratio.</li> </ul>	2.8 to 4.5		5.3	13.5	
	IDDOP(2)		<ul> <li>FmCF=8MHz ceramic oscillation mode</li> <li>FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	4.5 to 5.5		6.7	14	
	IDDOP(3)		<ul> <li>System clock set to 8MHz side</li> <li>Internal RC oscillation stopped</li> <li>frequency variable RC oscillation stopped</li> <li>1/1 frequency division ratio.</li> </ul>	2.5 to 4.5		3.8	10	
	IDDOP(4)		<ul> <li>FmCF=4MHz ceramic oscillation mode</li> <li>FmX'tal=32.768kHz by crystal oscillation mode</li> <li>System clock set to 4MHz side</li> </ul>	4.5 to 5.5		2.7	6	mA
	IDDOP(5)		<ul> <li>Internal RC oscillation stopped</li> <li>frequency variable RC oscillation stopped</li> <li>1/1 frequency division ratio.</li> </ul>	2.2 to 4.5		1.45	3.8	
	IDDOP(6)		<ul> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	4.5 to 5.5		0.95	4.3	
	IDDOP(7)		<ul> <li>System clock set to internal RC oscillation</li> <li>frequency variable RC oscillation stopped</li> <li>1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		0.53	3.0	
	IDDOP(8)		<ul> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz by crystal oscillation mode.</li> </ul>	4.5 to 5.5		1.25	5.2	
	IDDOP(9)		<ul> <li>System clock set to 1MHz with frequency variable RC oscillation</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		0.67	4.2	
	IDDOP(10)		FmCF=0Hz (oscillation stopped)     FmX'tal=32.768kHz by crystal oscillation     mode.     Created state state 20.760kHz side	4.5 to 5.5		38	110	
	IDDOP(11)		<ul> <li>System clock set to 32.768kHz side.</li> <li>Internal RC oscillation stopped</li> <li>frequency variable RC oscillation stopped</li> <li>1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		19	70	μA
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3	<ul> <li>HALT mode</li> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	4.5 to 5.5		3.2	7.5	
			<ul> <li>System clock set to 12MHz side</li> <li>Internal RC oscillation stopped</li> <li>frequency variable RC oscillation stopped</li> <li>1/1 frequency division ratio.</li> </ul>	2.8 to 5.5		1.8	4	
	IDDHALT(2)		HALT mode     FmCF=8MHz ceramic oscillation mode     FmX'tal=32.768kHz by crystal oscillation     mode	4.5 to 5.5		2.4	5.3	mA
	IDDHALT(3)		<ul> <li>System clock set to 8MHz side</li> <li>Internal RC oscillation stopped</li> <li>frequency variable RC oscillation stopped</li> <li>1/1 frequency division ratio.</li> </ul>	2.5 to 4.5		12.5	2.8	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

Continued on next page.

Parameter Symbol Pins/Remarks Conditions			Conditions			Specifi	cation	
- alamotor	0,			V <sub>DD</sub> [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(4)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3	<ul> <li>HALT mode</li> <li>FmCF=4MHz ceramic oscillation mode</li> <li>FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	4.5 to 5.5		1	2.3	
	IDDHALT(5)		<ul> <li>System clock set to 4MHz side</li> <li>Internal RC oscillation stopped</li> <li>frequency variable RC oscillation stopped</li> <li>1/1 frequency division ratio.</li> </ul>	2.2 to 4.5		0.5	1.3	
	IDDHALT(6)		HALT mode     FmCF=0Hz (oscillation stopped)     FmX'tal=32.768kHz by crystal oscillation     mode	4.5 to 5.5		0.33	0.9	mA
	IDDHALT(7) • System clock set to internal RC oscillation • frequency variable RC oscillation stopped • 1/2 frequency division ratio.					0.17	0.7	
	IDDHALT(8) • HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode.		4.5 to 5.5		1	3.8		
	IDDHALT(9)		<ul> <li>System clock set to 1MHz with frequency variable RC oscillation</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		0.5	2.7	
	IDDHALT(10)		<ul> <li>HALT mode</li> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz by crystal oscillation mode.</li> </ul>	4.5 to 5.5		18	70	
	IDDHALT(11)		<ul> <li>System clock set to 32.768kHz side.</li> <li>Internal RC oscillation stopped</li> <li>frequency variable RC oscillation stopped</li> <li>1/2 frequency division ratio.</li> </ul>	2.2 to 4.5		5	63	μА
HOLD mode	IDDHOLD(1)	V <sub>DD</sub> 1	HOLD mode	4.5 to 5.5		0.03	18	
consumption current	IDDHOLD(2)	1	<ul> <li>CF1=V<sub>DD</sub> or open (External clock mode)</li> </ul>	2.2 to 4.5		0.01	14	
Timer HOLD mode	IDDHOLD(3)		Timer HOLD mode     CF1=V <sub>DD</sub> or open (External clock mode)	4.5 to 5.5		16	63	
consumption current	IDDHOLD(4)		<ul> <li>FmX'tal=32.768kHz by crystal oscillation mode</li> </ul>	2.2 to 4.5		3.5	50	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

<b>F-ROM Programming Characteristics</b> at $Ta = +10^{\circ}C$ to $+55^{\circ}C$	Ζ,	VSS1 =	$V_{SS2} = 1$	VSS3 = 0V
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Demonster	Symbol	Dine/Demostra	Conditions		Specification				
Parameter	Symbol	Pins/Remarks Conditions	V <sub>DD</sub> [V]	min	typ	max	unit		
Onboard programming current	IDDFW(1)	V <sub>DD</sub> 1	Without CPU current	2.70 to 5.5		5	10	mA	
Programming	tFW(1)		• Erasing	2.7 to 5.5		20	30	ms	
time	tFW(2)		programming	2.7 to 5.5		40	60	μS	

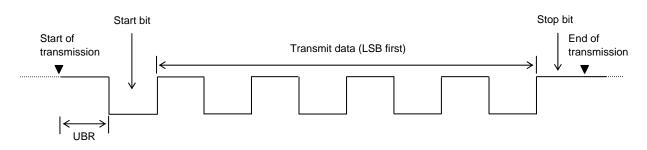
Deremeter	Sympol	Dine/Demorke	Conditions		Specification				
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Transfer rate	UBR	P32 (UTX1),							
		P33 (URX1),		2.5 to 5.5	16/3		8192/3	tCYC	
		P34 (UTX2),		2.5 to 5.5			0192/3	1010	
		P35 (URX2)							

Data length : 7/8/9 bits (LSB first)

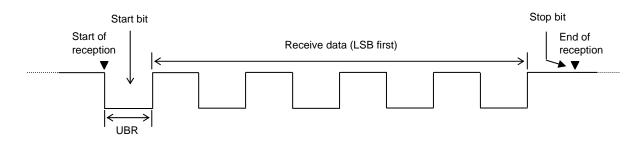
Stop bits : 1-bit (2-bit in continuous data transmission)

Parity bits : None

#### Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



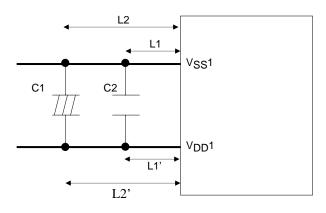
Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



## VDD1, VSS1 Terminal Condition

It is necessary to place capacitors between  $V_{DD}1$  and  $V_{SS}1$  as describe below.

- Place capacitors as close to  $V_{DD}1$  and  $V_{SS}1$  as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L1 = L1', L2 = L2').
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- $\bullet$  Capacitance of C2 must be more than  $0.1 \mu F.$
- $\bullet$  Use thicker pattern for VDD1 and VSS1.



#### **Characteristics of a Sample Main System Clock Oscillation Circuit**

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Nominal Vendor				Circuit C	constant		Operating Voltage		lation tion Time	Damadua						
Frequency	Name	Oscillator Name	C1	C2	Rf1	Rd1	Range	typ	max	Remarks						
			[pF]	[pF]	[Ω]	[Ω]	[V]	[ms]	[ms]							
12MHz		CSTCE12M0G52-R0	(10)	(10)	Open	470	2.6 to 5.5	0.05		Internal C1,C2						
		CSTCE10M0G52-R0	(10)	(10)	Open	470	2.4 to 5.5	0.05		Internal C1,C2						
10MHz								CSTLS10M0G53-B0	(15)	(15)	Open	680	2.6 to 5.5	0.05		Internal C1,C2
01411-	MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	680	2.3 to 5.5	0.05		Internal C1,C2						
8MHz		CSTLS8M00G53-B0	(15)	(15)	Open	1k	2.5 to 5.5	0.05		Internal C1,C2						
45.41.1-		CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.05		Internal C1,C2						
4MHz		CSTLS4M00G53-B0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.05		Internal C1,C2						

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after  $V_{DD}$  goes above the operating voltage lower limit (see Fig. 4).

### Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYOdesignated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

	usie 2 Characteristics of a Sample Subsystem Clock Obernator Chean whith a Crystar Obernator												
Nominal	Vendor	Oscillator Name		Circuit C	Constant		Operating Voltage		lation tion Time	Remarks			
Frequency	Name	Oscillator Name	C3	C4	Rf2	Rd2	Range [V]	typ	max	Remarks			
			[pF]	[pF]	[Ω]	[Ω]	[v]	[s]	[s]				
32.768kHz	SEIKO TOYOCOM	MC-306	18	18	Open	560k	2.2 to 5.5	1.2	3.0	Applicable CL value=12.5pF			

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure. 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

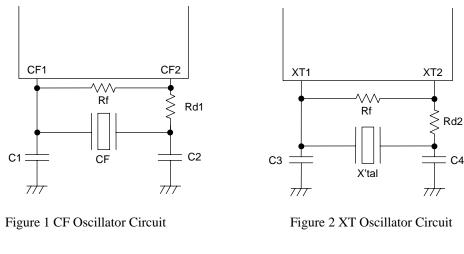
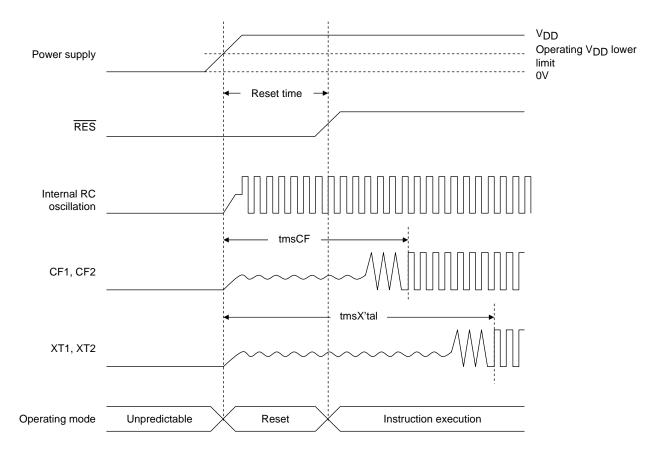
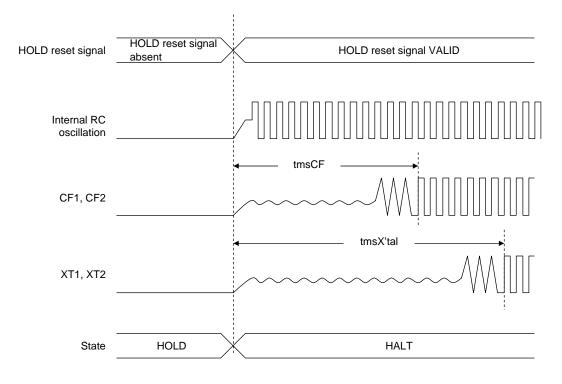




Figure 3 AC Timing Measurement Point

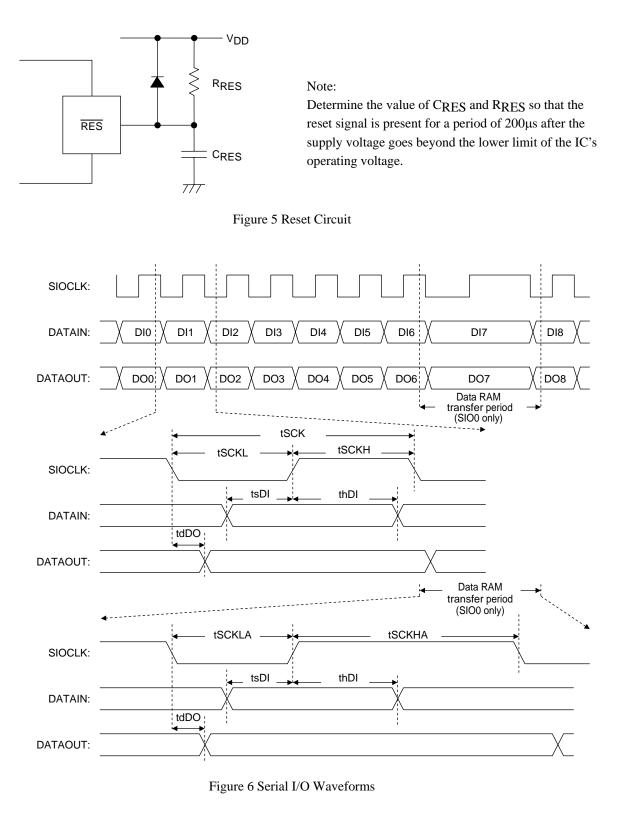


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



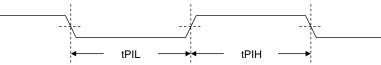


Figure 7 Pulse Input Timing Signal Waveform

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